**Listing of Claims**:

1. (Currently Amended) A method for predicting the timing response of a circuit path, the method comprising:

receiving a circuit block netlist;

obtaining a first estimated timing response of a first circuit path of [[a]] said circuit block ~~design~~ netlist using a first timing model;

obtaining a second estimated timing response of the first circuit path of ~~the same~~ said circuit block ~~design~~ netlist using a second timing model;

generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response; and

applying the correction factor to the first timing model.

2. (Original) The method as in claim 1 further comprising obtaining estimated timing responses of a plurality of circuit paths using the first timing model.

3. (Original) The method as in claim 2 further comprising:

selecting the first circuit path from the plurality of circuit paths, wherein applying the correction factor to the first timing model includes adjusting the estimated timing responses of the plurality of circuit paths based on the correction factor.

4. (Cancelled)

5. (Cancelled)

6. (Original) The method as in claim 1, wherein generating a correction factor includes comparing the first estimated timing response and the second estimated timing response.

7. (Original) The method as in claim 1, wherein applying the correction factor includes adjusting the first estimated timing response based on the correction factor.

8. (Original) The method as in claim 1, wherein the first estimated timing response includes an estimated signal propagation delay.

9. (Original) The method as in claim 1, wherein the first estimated timing response includes an estimated signal propagation time.

10. (Original) The method as in claim 1, wherein the correction factor includes a scaling factor.

11. (Original) The method as in claim 1, wherein the correction factor includes an offset.

12. (Currently Amended) A method for predicting the timing response of a circuit path, the method comprising:

obtaining coarse estimated timing responses for a plurality of circuit paths of a circuit block ~~design~~ netlist using a first timing model, the first timing model having a first accuracy;

obtaining refined estimated timing responses for one or more selected circuit paths of the plurality of circuit paths of ~~the same~~ said circuit block ~~design~~ netlist using a second timing model having a second accuracy greater than the first accuracy;

generating a correction factor based on the estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths; and

adjusting the coarse estimated timing responses of the plurality of circuit paths based on the correction factor.

13. (Original) The method as in claim 12, wherein obtaining the coarse estimated timing responses includes estimating timing responses for the plurality of circuit paths using a modeling tool employing coarse timing assumptions.

14. (Original) The method as in claim 12, wherein obtaining refined estimated timing responses includes using a modeling tool employing refined timing assumptions.

15. (Currently Amended) The method as in claim 12, further comprising generating [[a]] the circuit block netlist describing the plurality of circuit paths.

16. (Original) The method as in claim 12, wherein generating a correction factor includes determining a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths.

17. (Previously Presented) The method as in claim 16, further comprising:

generating a correction factor for each of the plurality of circuit paths, wherein the statistical variation is equal to a standard deviation of the correction factors for the plurality of circuit paths divided by mean of the correction factors for the plurality of circuit paths; and

adjusting the coarse estimated timing responses of each of the plurality of circuit paths individually, if the statistical variation exceeds twenty percent.

18. (Original) The method as in claim 12, wherein the coarse estimated timing responses include an estimated signal propagation delay.

19. (Original) The method as in claim 12, wherein the coarse estimated timing responses include an estimated signal propagation time.

20. (Original) The method as in claim 12, wherein the correction factor includes a scaling factor.

21. (Original) The method as in claim 12, wherein the correction factor includes an offset.

22. (Currently Amended) A method for generating a circuit design comprising:

obtaining a first estimated timing response of a first circuit path of a circuit block ~~design~~ netlist using a first timing model;

obtaining a second estimated timing response of the first circuit path of ~~the same~~ said circuit block ~~design~~ netlist using a second timing model;

generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response;

applying the correction factor to the first timing model to generate a corrected timing response; and

generating a circuit design using the corrected timing response.

23. (Previously Presented) The claim 22 further comprising obtaining estimated timing responses of a plurality of circuit paths using the first timing model.

24. (Previously Presented) The method claim 23, wherein applying the correction factor to the first timing model includes adjusting the first estimated timing response based on the correction factor.

25. (Previously Presented) The method of claim 23 further comprising:

selecting the first circuit path from the plurality of circuit paths, wherein applying the correction factor to the first timing model includes adjusting the estimated timing responses of the plurality of circuit paths based on the correction factor.

26. (Cancelled)

27. (Cancelled)

28. (Previously Presented) The method claim 22, wherein generating a correction factor includes comparing the first estimated timing response and the second estimated timing response.

29. (Cancelled)

30. (Currently Amended) A computer readable medium tangibly embodying a program of instructions, the program of instructions comprising:

at least one instruction executable to obtain coarse estimated timing responses for a plurality of circuit paths of a circuit block ~~design~~ netlist using a first timing model, the first timing model having a first accuracy;

at least one instruction executable to obtain a refined estimated timing response for a selected circuit path of the plurality of circuit paths of ~~the same~~ said circuit block ~~design~~ netlist using a second timing model having a second accuracy greater than the first accuracy;

at least one instruction executable to generate a correction factor based on the course estimated timing response of the selected circuit path and the refined timing estimate of the selected circuit path; and

at least one instruction executable to adjust the coarse estimated timing responses of the plurality of circuit paths based on the correction factor.

31. (Original) The computer readable medium as in claim 30, wherein the at least one instruction executable to obtain the coarse estimated timing responses includes at least one instruction executable to estimate timing responses for the plurality of circuit paths using a modeling tool employing coarse timing assumptions.

32. (Original) The computer readable medium as in claim 30, wherein the at least one instruction executable to obtain refined estimated timing responses includes at least one instruction to use a modeling tool employing refined timing assumptions.

33. (Currently Amended) The computer readable medium as in claim 30, further comprising at least one instruction executable to generate [[a]] the circuit block netlist describing the plurality of circuit paths.

34. (Original) The computer readable medium as in claim 30, wherein the at least one instruction executable to generate a correction factor includes at least one instruction to determine a statistical variation between the course estimated timing response of the one or more selected circuit paths and the refined timing estimates of the one or more selected circuit paths.

35. (Previously Presented) The computer readable medium as in claim 34, further comprising:

at least one instruction to generate a correction factor for each of the plurality of circuit paths, wherein the statistical variation is equal to a standard deviation of the correction factors for the plurality of circuit paths divided by mean of the correction factors for the plurality of circuit paths; and

at least one instruction to adjust the coarse estimated timing responses of each of the plurality of circuit paths individually, if the statistical variation exceeds twenty percent.

36. (Previously Presented) The computer readable medium as in claim 30, wherein the computer readable medium is selected from a group consisting of a random access memory, a read only memory, a magnetic tape, a magnetically encodable disk, an optically encodable tape, and an optically encodable disk.

37. (Currently Amended) A system for predicting the timing response of a circuit path, the method comprising:

first timing model means for obtaining a first estimated timing response of a first circuit path of a circuit block ~~design~~ netlist;

second timing model means for obtaining a second estimated timing response of the first circuit path of ~~the same~~ said circuit block ~~design~~ netlist;

correction factor generation means for generating a correction factor based on a variation between the first estimated timing response and the second estimated timing response; and

application means for applying the correction factor to the first timing model.

38. (Original) The system as in claim 37 wherein the first timing model means is further for obtaining estimated timing responses of a plurality of circuit paths.

39. (Original) The system as in claim 38 further comprising:

selection means for selecting the first circuit path from the plurality of circuit paths, wherein the application means adjusts the estimated timing responses of the plurality of circuit paths based on the correction factor.

40. (Currently Amended) The system as in claim [[38]] 37, further comprising a netlist means for generating [[a]] the circuit block netlist describing the plurality of circuit paths.

41. (Original) The system as in claim 37, wherein the correction factor generation means compares the first estimated timing response and the second estimated timing response.

42. (Original) The system as in claim 37, wherein the application means adjusts the first estimated timing response based on the correction factor.